This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-20 (cancelled)

21. (new)   A method of managing performance in a system, comprising:
monitoring a time related level of processing activity by a processing unit including a processor, and

increasing or decreasing the performance level of the processor according to the monitored level of processing activity.

22. (new)   A method according to claim 21, wherein the processor activity is determined by monitoring input/output operations associated with the processor.

23. (new)   A method according to claim 22, wherein the input/output operations comprise write cycles.

24. (new)   A method according to claim 21, wherein the processor activity is determined by monitoring accesses by the processor to memory coupled to the processor.

25. (new)   A method of processor performance management, comprising:
monitoring a time related level of processing activity by a processing unit, and
increasing or decreasing processor performance level of the processing unit according to the monitored level of processing activity.

26. (new)   A method according to claim 25, wherein the processor activity is determined by monitoring input/output operations by the processor.

27. (new)   A method according to claim 26, wherein the input/output operations comprise write cycles.

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28. (new)   A method of computer performance management, comprising:

monitoring a time related level of processor activity in a CPU involving selected memory access operations, and

increasing or decreasing the CPU processor performance level according to the monitored level of processing activity.

29. (new)   A method according to claim 28, wherein the processor activity is determined by monitoring accesses by the processor to memory coupled to the processor.

30. (new)   A method according to claim 28, wherein the monitored memory access operations comprise cache memory read misses and write operations.

31. (new)   A computer system comprising:

a processor;

memory coupled to the processor;

a monitor operable to determine processor activity level based on selected processor access operations associated with said memory;

circuitry operable to increase or to decrease processor performance level in response to the monitored level of processor activity changing from a threshold.

32. (new)   A computer system according to claim 31, including cache memory coupled to the processor, and wherein said monitor is operable to monitor cache hits to determine processor activity level.

33. (new)   A computer system according to claim 31, including cache memory coupled to the processor, and wherein said monitor is operable to monitor cache memory read misses and write operations to determine processor activity.

34. (new)   A computer system comprising:

a processor;

a plurality of devices coupled to the processor;

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a monitor operable to determine processor activity level based on selected processor input/output operations associated with at least one of said devices;

circuitry operable to increase or to decrease processor performance level in response to the monitored level of processor activity changing from a threshold.

35. (new)   A computer system according to claim 34, including a counter to count the monitored selected processor input/output operations.

36. (new)   A computer system comprising:

a processor;

memory coupled to the processor;

a plurality of devices coupled to the processor;

a monitor operable to determine processor activity level based on selected processor input/output operations associated with at least one of said devices and selected memory access operations by the processor;

circuitry operable to increase or to decrease processor performance level in response to the monitored level of processor activity changing from a threshold.

37. (new)   A computer system according to claim 36, wherein the selected memory access operations include cache memory access operations.

38. (new)   A computer system according to claim 37, wherein the selected memory access operations include cache memory read misses and write operations.

39. (new)   A computer system according to claim 36, including a plurality of counters for separately recording the selected processor input/output operations and the selected memory access operations.

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